

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-20. (Cancelled)

21. (New) A circuit for testing a transceiver, comprising:

a test pattern generator generating a first test pattern and a second test pattern;

a multiplexer having a first input, a second input, and an output, the first input receiving the first test pattern and the second input receiving the second test pattern;

a demultiplexer having an input, a first output, and a second output, the input of the demultiplexer being coupled to the output of the multiplexer; and

a test result evaluation circuit generating a first signature based on a first data stream generated by the first output of the demultiplexer and a second signature based on a second data stream generated by the second output of the demultiplexer, the test result evaluation circuit comparing each generated signature to a stored signature for determining whether an error has occurred during the transmission of an associated data stream.

22. (New) The circuit of claim 21, wherein the first test pattern is different from the second test pattern.

23. (New) The circuit of claim 21, wherein the first signature is equal to the second signature.

24. (New) The circuit of claim 21, wherein the test result evaluation circuit further includes:

a controller identifying a start of a particular data stream; and

a recorder recording the data stream in response to the identification.

25. (New) The circuit of claim 24, wherein the start of the particular data stream is identified based on an identification of a specific bit sequence in the data stream.

26. (New) The circuit of claim 24, wherein a particular signature is generated based on the recorded data stream.

27. (New) The circuit of claim 21 further comprising:

a selector coupled to the multiplexer, the selector selecting between an input signal data, and the first and second test patterns generated by the test pattern generator.

28. (New) The circuit of claim 21, wherein the selector selects the first and second test patterns during a testing mode, and the input signal data during a non-testing mode.

29. (New) The circuit of claim 21, wherein the circuit is integrated within the transceiver circuitry.

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30. (New) A circuit for testing a transceiver, comprising:

means for generating a first test pattern and a second test pattern;

a multiplexer having a first input, a second input, and an output, the first input receiving the first test pattern and the second input receiving the second test pattern;

a demultiplexer having an input, a first output, and a second output, the input of the demultiplexer being coupled to the output of the multiplexer; and

means for generating a first signature based on a first data stream generated by the first output of the demultiplexer and a second signature based on a second data stream [from] generated by the second output of the demultiplexer;

means for comparing each generated signature to a stored signature; and

means for determining, based on the comparison, whether an error has occurred during the transmission an associated data stream.

31. (New) The circuit of claim 30, wherein the first test pattern is different from the second test pattern.

32. (New) The circuit of claim 30, wherein the first signature is equal to the second signature.

33. (New) The circuit of claim 30 further comprising:

means for identifying a start of a particular data stream; and

means for recording the data stream in response to the identification.

34. (New) The circuit of claim 33, wherein the start of the particular data stream is identified based on an identification of a specific bit sequence in the data stream.

35. (New) The circuit of claim 33, wherein the means for generating a signature generates a particular signature based on the recorded data stream.

36. (New) The circuit of claim 30 further comprising:  
means for selecting between an input signal data, and the first and second test patterns generated by the test pattern generator.

37. (New) The circuit of claim 30, wherein the means for selecting selects the first and second test patterns during a testing mode, and the input signal data during a non-testing mode.

38. (New) The circuit of claim 30, wherein the circuit is integrated within the transceiver circuitry.